

Form PTO-1449 (modified) List of Patents and Publications For Applicant's Information Disclosure Statement (Use several sheets if necessary)	FEB 27 2001 RECEIVED PATENT & TRADEMARK OFFICE	DKT. NO.: P5826 US APPLICANTS: Lee et al. FILING DATE: September 28, 2001	SERIAL NO.: 09/967,142 GROUP: unknown 2663
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U.S. PATENT DOCUMENTS

EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
W	A1	6,016,510	1/18/00	Quattromani, et al.			
W	A2	6,023,753	2/8/00	Pechanek, et al.			
W	A3	5,689,661	11/18/97	Hayashi, et al.			
W	A4	6,167,502	12/26/00	Pechanek, et al.			
W	A5	6,101,181	8/8/00	Passint, et al.			
W	A6	5,720,025	2/17/98	Wilkes, et al.			
W	A7	5,970,232	10/19/99	Passint, et al.			
W	A8	6,055,618	4/25/00	Thorson			
W	A9	5,701,416	12/23/97	Thorson, et al.			
W	A10	5,737,628	4/7/98	Birritella, et al.			
W	A11	5,689,646	11/18/97	Thorson			

FOREIGN PATENT DOCUMENTS

EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
W	A12	99/26429	5/27/99	WO			
W	A13	0 785 512	7/23/97	EP			

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

W	A14	Bradley Kuszmaul, Mercury Computer Systems, Inc., "The RACE Network Architecture," (posted at www.mc.com/techlit/#tech_brief prior to this), 6 pages.
W	A15	R.Y. Wang, T.E. Anderson and D.A. Patterson, "Virtual Log Based File Systems For a Programmable Disk," Proc. Third Symposium on Operating Systems Design and Implementation, February 1999 (Also appeared as University of California Technical Report CSD-98-1031, 16 pages.
W	A16	Prasant Mohapatra, "Wormhole Routing Techniques for Directly Connected Multicomputer Systems, ACM Computing Surveys, Vol. 30, No. 3, September 1998, 37 pages.
W	A17	Christopher Glass and Lionel Ni, "The Turn Model for Adaptive Routing," Journal of the Association for Computing Machinery, Vol. 41, No. 5, September 1994, pp. 874-902.

EXAMINER: *Christina*

DATE CONSIDERED: 4/27/05

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the patent owner.

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OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)			
ω	A18	Reddy, Dept. of Computer & Information Sciences, "A Dynamically Reconfigurable WDM LAN Based on Reconfigurable Circulant Graph," IEEE, 1996, 4 pages.	
ω	A19	Funahashi, Jouraku and Amano, "Adaptive Routing for Recursive Diagonal Torus," Transactions of the Institute of Electronics, Information and Communication Engineers D-I, vol. J83D-I, no. 11, November 2000, pp. 1143-53.	
ω	A20	Milan Kovacevic, Center for Telecommunications Research, "On Torus Topologies with Random Extra Links," IEEE 1996, pp. 410-418.	
ω	A21	Dally, et al., The Torus Routing Chip, Distributed Computing, Springer-Verlag 1986, pp. 187-196.	
ω	A22	Susan Hinrichs, "A Compile Time Model for Composing Parallel Programs," IEEE Parallel and Distributed Technology, 1995, 19 pages.	
ω	A23	"CRAY T3D System Architecture Overview Manual," ftp://ftp.cray.com/product-info/mpp/T3D_Architecture_Over/T3D.overview.html, Cray Research, 1993, 40 pages.	
ω	A24	Marco Fillo, et al., "The M-Machine Multicomputer," Laboratory for Computer Science, Massachusetts Institute of Technology, A.I. Memo No. 1532, Ann Arbor, March 1995, 14 pages.	
ω	A25	Noakes, et al., "The J-Machine Multicomputer: An Architectural Evaluation," Proceedings of the 20 th International Symposium on Computer Architecture, May 1993, 12 pages.	
ω	A26	Dally, et al., "Architecture of a Message-Driven Processor," International Conference on Computer Architecture, June 1987, pp. 189-196.	
ω	A27	Dennison, Lee and Dally, "High-Performance Bidirectional Signalling in VLSI," Massachusetts Institute of Technology, October 12, 1992, 20 pages.	
ω	A28	Dally, et al., "Architecture and Implementation of the Reliable Router," Mass. Institute of Technology, Proceedings of Hot Interconnects II, Stanford CA, August 1994, 12 pages.	
ω	A29	Dally, et al., "The Reliable Router: A Reliable and High-Performance Communication Substrate for Parallel Computers," Proceedings of the First International Parallel Computer Routing and Communication Workshop, Seattle WA, May 1994, 15 pages.	
ω	A30	Dennison, et al., "Low-Latency Plesiochronous Data Retiming," Mass. Institute of Technology, Proceedings of the 1995 Advanced Research in VLSI Conference, Chapel Hill NC, March 1995, 12 pages	
ω	A31	Whay S. Lee, "Mechanism for Efficient, Protected Messaging," Massachusetts Institute of Technology, Dept. of Electrical Engineering and Computer Science, January 20, 1999, 147 pages.	
ω	A32	Dennison, "Reliable Interconnect Networks for Parallel Computers," Mass. Institute of Technology, Dept. of Electrical Engineering and Computer Science, April 18, 1991, 79 pages.	
ω	A33	Thucydides Xanthopoulos, "Fault Tolerant Adaptive Routing in Multicomputer Networks," Dept. of Electrical Engineering and Computer Science, Mass. Institute of Technology, January 20, 1995, 152 pages.	
ω	A34	Dennison, "The Reliable Router: An Architecture for Fault Tolerant Interconnect," Dept. of Electrical Engineering and Computer Science, Mass Institute of Technology, May 24, 1996, 145 pages.	

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